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# Optimization Of Low Power Digital Vlsi Using High Speed Sram

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## ABSTRACT

Today's mobile communication devices are equipped with large-capacity memory in order to accommodate all of their customers' multimedia needs. Providing high-bandwidth and low-power memory are the primary concerns of today's design engineers. In this post, we've constructed a low-power SRAM cell by modifying the Multi-threshold CMOS architecture. CMOS transistors with different threshold voltages may be used to reduce power consumption and delay. This study suggests an exciting technique to decrease leakage current in idle state to reduce power usage. These three variables—voltage, temperature, and transistor size—all have an impact on how much power an SRAM cell consumes when tested this way. To reduce the memory structure's power consumption, a novel SRAM cell design has been proposed in this work. Comparatively speaking, the 45 nm SRAM cell is smaller than a normal 6T SRAM module. There is a 21% reduction in power consumption when compared to conventional 6T SRAM architectures, according to simulations.

**KEYWORDS:** Tanner EDA, CMOS design, Static Power, Power gating.

## INTRODUCTION

When designing for extremely large scale integration, it is essential to take increased power consumption, transistor density, CMOS size scaling into account (VLSI). Both dynamic and static power dissipation are included in CMOS circuit power dissipation. When the system is running, the circuit generates dynamic power. A CMOS circuit's

switching and short-circuiting power requirements are well understood. When the load capacitance (CL) is charged and drained, short circuit power dissipation occurs. As a result of these and other leakage power dissipation mechanisms, the main source of heat generation in semiconductor devices is the sub threshold leakage. The total power consumption of the CMOS circuit is increased as a result of increasing the leakage current in the devices.

A mobile device's battery life is determined by the amount of leakage that occurs when it is in sleep mode. In CMOS circuits, a range of urbanised static approaches may minimise the amount of static current. In the current circumstance, static power may be reduced utilising NMOS footers or PMOS headers with high threshold voltages. In order to limit the amount of switching energy, a unique power gating with charge recycling technology may be used. In both sleep-in and active modes, switching power is split between a virtual VDD and a virtual VSS line. The virtual VDD and VSS lines are connected to the power and ground supply, respectively, via PMOS and NMOS switches. A system that uses charge recycling even while in sleep mode can lose more energy than one that does not. Because it takes longer for the charge recycled power gating to balance the virtual VDD and VSS lines, the wake-up time is longer.

## LITERATURE REVIEW

**SUDHAKAR ALLURI, B. BALAJI AND CH. CURY (2021)** FINFET-based static RAM cells with six transistors have been built and simulated in this work, and the design problems and achievement metrics of advanced SRAM cells are then examined. SCEs have been minimised, the allowable duration has been cut to an ultra-small value, and the Hugh stability of this operation with a low power domain has been evaluated. At the 45nm node, FINFET 6 Transistor Static RAM was compared to MOSFET 6 Transistor Static RAM for leakage current, static noise margin, sub threshold current and power dissipation. After the leakage current and power consumption have been greatly decreased, the same procedure is used to updated SRAM cells. SRAM cells with FINFET have been compared to normal advanced MOSFET with Static RAM cells in terms of performance.

**M.SRINIVAS1 AND DR.K.V.DAYA SAGA (2021)** Leakage currents, which are increasing at an alarming rate, are the primary source of power waste in idle mode. The scaling of the threshold voltage causes a rise in gate current leakage, which in turn causes a rise in sub-threshold leakage. Leakage energy consumption has gained increasingly more attention as the demand for mobile devices grows. When a mobile device spends most of its time in standby mode, leakage power reductions are necessary to increase the battery life. As a result, power consumption has become an increasingly important consideration in CMOS circuit design. Design and simulation of an AND gate using the MOS parameter model at 27 0C, 0,70V supply voltage using 65nm CMOS technology validates the proposed circuit. In the context of conversation, of course. On the other hand, current MTCMOS and SCCMOS techniques are compared

in terms of leaky power dissipation in active and sleep modes as well as dynamic dissipation and propagation duration.

**HEMANT KUMAR (2021)** Reverse logic SRAM (RL-SRAM) is demonstrated at 32 nm, with Add 0.7 V, together with RL-SRAM with body bias in this study. Node capacitance energy may be reused rather than dissipated as heat in SRAM cells with reversible logic that use the adiabatic technique. The delay improvement achieved by CNTFET RL-SRAM and body biassed RL-SRAM when compared to CNTFET SRAM cells is 60.72 percent and 65.20 percent, respectively. A comparison with previous work shows that the CNTFET SRAM cell design significantly improves average power consumption, delay time, and leakage power dissipation without affecting the overall performance of the system. The memory cell's stability is further tested using butterfly curve and N-curve analysis.

**S POUSIA1AND K MURUGAN (2021)** Low-power, high-speed CMOS device design is one of today's toughest problems. As technology advances, static power consumption poses a growing challenge. There are many methods for minimising leakage power that include the sleep technique, stack technique, sleepy stack, sleepy keeper technique, leakage control transistor technique (LECTOR) and sleepy keeper leakage control transistor technique (SK-LCT). The CMOS architecture was able to achieve low power consumption and high speed using the suggested power gating approach. This approach is used to define the x or gate, x nor gate, half adder, and 6T SRAM cell in an energy efficient, high-speed architecture. SRAM cells use 14.29 percent less power and 34.37 percent less delay than a half adder, which saves 35.9 percent and 25.69 percent, whereas x or gate uses 19.5% less power and 33.5 percent less delay. Nor gate uses 12.5% less power and 23.29 percent less delay. Tanner's EDA tool dramatically reduces leakage power usage and simulation speed.

**HEMANT KUMAR, SUBODH SRIVASTAVA, (2017)** Power dissipation in the NANO scale range has become a major issue due to the persistent advancement of silicon technology. It is possible to reduce the amount of power used in a digital system while simultaneously increasing the system's performance. Several low power CNTFET SRAM cells based on Cadence Virtuoso 32 nm technology are examined in this research for their performance. Sleep, Zigzag, Stack, Sleepy Keeper (SK), and Leakage Feedback are among the low-power methods used in the CNTFET SRAM cell in this study (SSK). The average power dissipation is reduced by 84.26 percent (81.13 percent) with sleepy keeper (leakage feedback with stack), the delay is reduced by 38.12 percent (43.01 percent), and the leakage power dissipation is reduced by 9.15 percent (20.80 percent) with sleepy keeper. A butterfly curve and analytic N-curve approach are used to assess the proposed CNTFET SRAM cells' memory cell stability, which is a major design restriction. System performance can be enhanced despite an increase in cell area, as the SRAM cell's performance indices improve dramatically.

## LOW POWER MEMORY DESIGN REQUIREMENT

Embedded systems' memory requirements have skyrocketed in recent years owing to the proliferation of multimedia data. 4G and 5G wireless improvements are largely responsible for this. The VLSI industry is increasing the memory capacity of digital systems in order to satisfy the needs of 4G and 5G technologies (Bushnell et al., 2004) A large portion of the die is occupied with memories, which take up more than half the area. Embedded systems need a lot of power because of this. VLSI circuits generate a lot of heat because of their high power consumption. Increasing electricity consumption necessitates the installation of more heat sinks in order to reduce the amount of heat generated. When new packaging techniques are required, more system expenses are incurred (Alfailakawi et al., 2015). The industry has developed methods to reduce power consumption during memory read and write cycles (Mai et al., 1998) (Karlsson et al., 2005). The read/write latency, power consumption, and circuit complexity are all taken into account simultaneously in this approach.

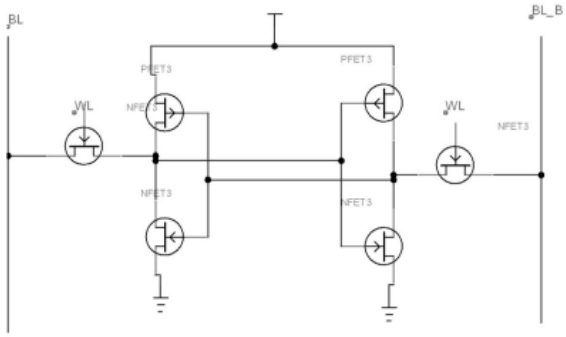


**Figure 1 "Schematic diagram of standard 6T SRAM cell"**

Cache memories use Static Random Access Memory (SRAM) as their primary memory storage. Figure 1 depicts a conventional 6T SRAM cell schematic. Low-power SRAM has a significant impact on any integrated circuit's power efficiency. Power consumption is reduced significantly as a consequence of technological scalability, as anticipated by Moore. Static leakage current has increased significantly due to scaling, though. The system's behavior changes when the technology scales beyond 10 nanometers. So, the design engineers are seeking for alternatives to technology scaling in order to build low-power systems.

## EXPERIMENTAL RESULTS

All SRAM architectures are shown in Table 1 with their total and static power consumption. As a comparison, we look at standard SRAM, Meritor-based SRAM, and the Proposal for a new SRAM design (based on MTCMOS). The proposed SRAM arrangement reduces total power and static power significantly, according to the findings of the comparisons. For both static and total power usage, Figure 4 provides a visual comparison of the various SRAM structures. At room temperature, these results were attained for a variety of SRAM architectures. Different SRAM designs are compared in Table 2 based on their power consumption at various temperatures. Figure

5 depicts the power consumption of several SRAM architectures at various temperatures. The power consumption of various SRAM architectures does not vary much at low temperatures, however the suggested structure has a large decrease at high temperatures.

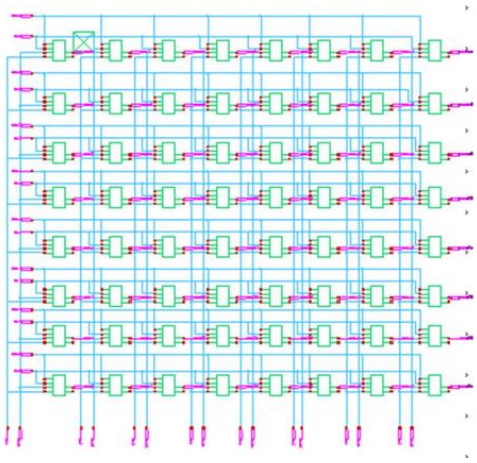

**Figure 2 8X8 SRAM schematic with proposed SRAM architecture**

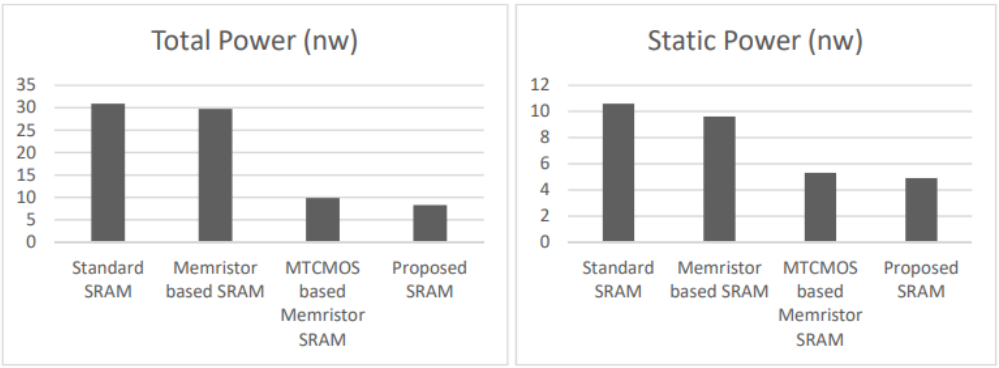


**Figure 3 "Comparison of total power and Static power for different SRAM structures"**

**Table 1 Total power and static power for different SRAM structure**

| SRAM | Voltage (v) | Total power (nw) | Static Power (nw) |
|---|---|---|---|
| Standard SRAM | 0.7 | 30.90 | 10.59 |
| Meritor based SRAM (Baghel et al., 2015) | 0.7 | 29.69 | 09.61 |
| MTCMOS based Memristor SRAM | 0.7 | 09.84 | 05.30 |
| Proposed SRAM | 0.7 | 08.28 | 04.89 |

**Table 2 Total power of different SRAM cells at different temperatures**

| SRAM | Temp 10°C nw | Temp 25°C nw | Temp 40°C nw | Temp 55°C Nw |
|---|---|---|---|---|
| Standard SRAM | 06.79 | 06.90 | 30.90 | 48.10 |
| MTCMOS SRAM | 04.90 | 06.43 | 09.84 | 18.12 |
| Proposed SRAM | 03.05 | 03.47 | 08.28 | 12.08 |

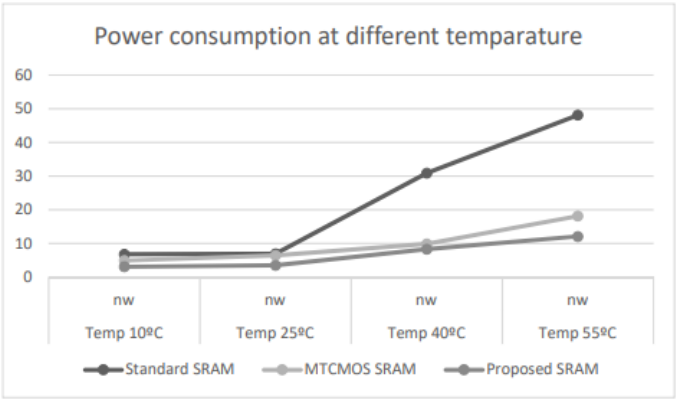


**Figure 4 "Graph representing power consumption of different SRAM structures"**

## CONCLUSIONS

A novel SRAM design architecture is presented in this research. Memory consumes two types of power: primary and secondary. Among the most important components are both static and dynamic power. Dynamic and static power are generated when cells are switched from 0 to 1 or 1 to 0, respectively, in idle mode. Total power consumption is heavily influenced by leakage current when transistors have a length and width of less than 75nm. A modified MTCMOS design has been presented as a way to minimise leakage current. At different temperatures, the new design is compared to a regular 6T SRAM build. At rated temperature, the suggested 8X8 SRAM architecture reduces power consumption by about 21% compared to the current architecture. Adopting double-gate CMOS devices can improve the currently proposed SRAM design even further.

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